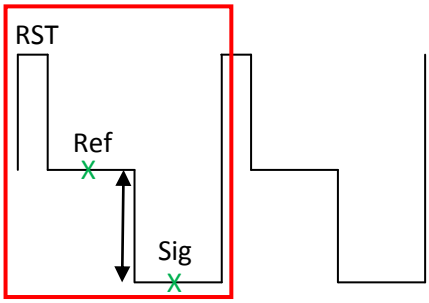
Technical Note

Digital Correlated Double Sampling (DCDS) on the iXon Ultra

The video output signal from a CCD has the following form:



In each pixel (defined by red box) both a reference measurement and a signal measurement are made to determine the level of charge within that pixel. This is done by simply calculating the difference between the measured reference and signal levels. A reset pulse is used at the beginning of each pixel to return the output to a defined level. This technique of Correlated Double Sampling (CDS) is performed digitally by the Field Programmable Gate Array (FPGA).

The iXon Ultra uses a 16-bit Analogue to Digital Convertor (ADC) to sample the analogue voltage output from the CCD in the range 0 to 65535 counts. As the CCD video output is passed through the ADC, analogue voltage units of signal and reference must be within the 16-bit range of the ADC. Therefore, after subtraction, the maximum digital number which can represent the charge accumulated within the pixel will always be less than 65535 counts. The magnitude of the dark offset can vary with a number of parameters, including horizontal shift rate, Preamp gain and EM gain, which will change the appearance of the CCD video output at the ADC. This is why differing saturation points are observed as these parameters change.

The iXon Ultra offers true 16-bit resolution, but it is not possible to display the entire 65535 count range with this sampling architecture. With the correct choice of exposure time, EM gain and Preamp gain, the performance of the camera is not compromised.

It is important to note that acquiring images at high signal levels with EM gain applied should be avoided. This will limit the life of your camera as the EM gain register will become irreparably damaged.